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09/620,140	07/20/2000	David A. Zimlich	2146-12	2828

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Nixon & Vanderhye PC
8th Floor
1100 North Glebe Rd
Arlington, VA 22201-4714

EXAMINER	
NGUYEN, JENNIFER T	
ART UNIT	**PAPER NUMBER**
2674	10

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/620,140	Applicant(s) ZIMLICH, DAVID A.	
	Examiner Jennifer T Nguyen	Art Unit 2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24,26-34 and 36* is/are rejected.

7)☒ Claim(s) *25 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to amendment filed on 12/29/2003.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 6, 7, 9, 10, 15, 16, 18, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Yasunishi et al. (U.S. Patent No. 6,597,335).

Regarding claims 1, 9, and 18, referring to Figs. 1 and 5, Yasunishi teaches a driver circuit for driving signal lines of a matrix type display device (8) comprising: pulsewidth modulation circuitry (5) for generating pulsewidth modulated video data (S501); and driver circuitry (7U) for latching (72) the pulsewidth modulated video data (S501) and driving said signal lines in accordance with the latched data (from col. 5, line 64 to col. 7, line 9 and from col. 8, line 51 to col. 9, line 2).

Regarding claims 2 and 10, Yasunishi further teaches the driver circuitry (7U) level-shifting the pulsewidth modulated video data (from col. 8, line 51 to col. 9, line 2).

Regarding claims 6, 15, and 21, Yasunishi further teaches the pulsewidth modulation circuitry (5) generates the pulsewidth modulated video data (S501) based on RGB video data supplied thereto (col. 9, lines 46-59).

Regarding claims 7 and 16, Yasunishi further teaches the driver circuitry (7U) is provided on a chip other than a chip on which said pulsewidth modulation circuitry (5) is provided (Fig. 1, col. 6, lines 54-67).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 4, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasunishi et al. (U.S. Patent No. 6,597,335) in view of Embry et al. (U.S. Patent No. 6,094,689).

Regarding claims 3, 4, 13, and 14, Yasunishi differs from claims 3, 4, 13 and 14 in that he does not specifically teach a programmable logic array and ASIC for pulsewidth modulation circuitry. However, Embry teaches that it is well known in the art to utilize a programmable logic array and ASIC for providing pulsewidth modulation circuitry (col. 24, lines 11-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the programmable logic array and ASIC for pulsewidth modulation circuitry as taught by Embry in the system of Yasunishi in order to simplify the circuitry and save space, reduce size, weight and costs.

6. Claims 5, 11, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasunishi et al. (U.S. Patent No. 6,597,335) in view of Suzuki et al. (U.S. Patent No. 6,580,407).

Regarding claims 5, 11, and 19, Yasunishi differs from claims 5, 11, and 19 in that he does not specifically teaches the signal lines are connected to emitter elements of a field

emission display. However, referring to Fig. 8, Suzuki teaches the signal lines are connected to emitter elements of a field emission display (from col. 10, line 34 to col. 11, line 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the field emission display as taught by Suzuki in the system of Yasunishi in order to provide a display device is simple to manufacture and even a device having a large area can be fabricated with ease and having a high picture quality.

7. Claims 8, 12, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasunishi et al. (U.S. Patent No. 6,597,335) in view of Takemori et al. (U.S. Patent No. 5,202,674).

Regarding claims 8 and 17, Yasunishi differs from claims 8 and 17 in that he does not specifically teach driver circuits that are loaded in parallel with the pulsewidth modulated video data. However, Takemori teaches driver circuits that are loaded in parallel with the pulsewidth modulated video data (Fig. 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the driver circuits that are loaded in parallel with the pulsewidth modulated video data as taught by Takemori in the system of Yasunishi in order to provide an easy and efficient data processing into the driver circuits.

Regarding claims 12 and 20, Yasunishi differs from claims 12 and 20 in that he does not specifically teach the matrix type display device is plasma display device. However, referring to Fig. 5, Takemori teaches the matrix type display device is plasma display device (col. 1, lines 56-62 and from col. 4, line 56 to col. 5, line 14). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the plasma display device as taught by Takemori in the system of Yasunishi in order to provide a display device is

simple to manufacture and even a device having thin, light weight, and high level of maximum brightness.

8. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasunishi et al. (U.S. Patent No. 6,597,335) in view of Hyun (U.S. Patent No. 6,144,374).

Regarding claim 22, referring to Figs. 1 and 5, Yasunishi teaches a driver circuit for driving signal lines of a matrix type display device (8) comprising: pulsewidth modulation circuitry (5) for generating pulsewidth modulated video data (S501); and driver circuitry (7U) for latching (72) the pulsewidth modulated video data (S501) and driving said signal lines in accordance with the latched data (from col. 5, line 64 to col. 7, line 9 and from col. 8, line 51 to col. 9, line 2).

Yasunishi differs from claim 22 in that he does not specifically teach an output transistors. However, referring to Figs. 2 and 7, Hyun teaches an output transistors (40) for driving said signal lines in accordance with the latched data (col. 5, lines 14-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the output transistors as taught by Hyun in the system of Yasunishi in order to provide an output driving circuit for enabling display gradation processing by control the amount of currents.

Regarding claim 23, Yasunishi further teaches a single latch circuit (72) is provided for each signal line (Fig. 6, from col. 8, line 51 to col. 9, line 2).

9. Claims 24 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasunishi et al. (U.S. Patent No. 6,597,335) in view of Hyun (U.S. Patent No. 6,144,374) and further in view of Holloman (U.S. Patent No. 5,796,375).

Regarding claim 24, the combination of Yasunishi and Hyun differs from claim 24 in that it does not specifically teach a data buffer whose outputs are selectively latched into the latch circuit in accordance with latch enable signals. However, referring to Fig. 9, Holloman teaches a data buffer (64) whose outputs are selectively latched into the latch circuit in accordance with latch enable signals (i.e., latch en) (from col. 4, line 56 to col. 5, line 12). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the data buffer as taught by Holloman in the system of the combination of Yasunishi and Hyun in other to allow the video signals are successively transferred to the latch circuit.

Regarding claim 34, the combination of Yasunishi, Hyun, and Holloman further teaches a plurality of registers each including a respective flip-flop (Figs. 14 and 15 of Hyun, col. 7, lines 51-58).

10. Claims 26-33, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasunishi et al. (U.S. Patent No. 6,597,335) in view of Holloman (U.S. Patent No. 5,796,375).

Regarding claims 26-30, Yasunishi differs from claims 26-30 in that he does not specifically teach a data buffer whose outputs are selectively latched into the latch circuit in accordance with latch enable signals. However, referring to Fig. 9, Holloman teaches a data buffer (64) whose outputs are selectively latched into the latch circuit in accordance with latch enable signals (i.e., latch en) (from col. 4, line 56 to col. 5, line 12). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the data buffer as taught by Holloman in the system of Yasunishi in other to allow the video signals are successively transferred to the latch circuit.

Regarding claims 31-33 and 36, the combination of Yasunishi and Holloman further teaches a plurality of multi-bit circuits (i.e., Red, Green, Blue latches) and respective enable signals (i.e., latch en) are provided to the multi-bit circuits to load the contents of the data buffer (64) therein.

11. Claims 25 and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. Applicant's arguments with respect to claims 1-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Jennifer T. Nguyen** whose telephone number is **703-305-3225.** The examiner can normally be reached on Mon-Fri from 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reach at **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to: 703-872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, sixth-floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the Technology Center 2600 Customer Service Office whose telephone number is 703-306-0377.

JNguyen
3/26/2004

REGINA LIANG
PRIMARY EXAMINER